Metal Assisted Chemical Etching (MacEtch)

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1. **Description**: This process can produce arrays of high aspect ratio nanowires, trenches and other 3D structures directly in silicon. Thin metal micro-/nano-scale patterns generated via the Center’s electrochemical stamping process (Solid-State Superionic Stamping, S4) or other nanoscale processes serve as a catalyst for this anisotropic wet etch process. The etching at the metal catalyst –Si contacts are greatly enhanced, resulting in the anisotropy of the process. Characteristics of the nanowire array such as diameter, spacing, length, and geometry, can be effectively controlled by process parameters such as etchant composition and temperature.

Recent developments include the use of a thin-film dewetting process to create a mesh with a thin Au film with a controlled distribution of diameters which in turn yields arrays of smooth silicon nanowires of varying diameters averaging from a minimum of 110 nm (standard deviation, 40 nm) to 500 nm depending on the initial film deposition rate and thickness.

2. **Resolution demonstrated**:
   - **Wires**: controllable ~ 1um to 30 nm diameter, lengths to >30 um
   - **Lines/trenches**: to ~100 nm wide, depths ~ 200 nm

3. **Geometric capabilities**: Arrays of 3D structures (wires, cones, pyramids, etc.)

4. **Materials**:
   - **Metal patterns tested**: silver, gold
b. **Substrates tested**: silicon

5. **Process**
   a. **Environment**: ambient temperatures and atmospheric pressure
   b. **Speed**: etch rate, 60nm/min – 1000 nm/min
   c. **Control**: Etch only occurs at the metal catalyst-Si contacts
   d. **Pattern fabrication**: easily fabricated 2D patterns in metals with S4, soft lithography, other processes

6. **Dimensional capabilities**: moderate, 20 um X 20um demonstrated

7. **Uniqueness**:
   a. Direct nanoscale patterning of silicon
   b. Wide variety of cross-section shapes easily produced

8. **Competition**:
   a. Reactive ion etch
   b. Chemical Vapor Deposition (CVD) processes

9. **Limitations**:
   a. Not suitable for multilayer situations
   b. Substrates limited

10. **IP Status**: Patents applied for

11. **Potential Applications**:
   a. Thermoelectrics
   b. Photovoltaics
   c. Photonics
   d. Low-k structures
   e. 3D Si metamaterial structures
   f. High emissivity surfaces
   g. Optoelectronic devices with group III-V materials substrates

12. **Current Research Focus**:
   a. Si etch control, etched Si geometry tuning
   b. Si-Ge alloy etch
   c. Embedded Au/Ag device construction
13. MacEtch Examples:
   a. Typical patterns

   Illustration showing creation of silicon pillars/nanowires from silver S4 produced metal pattern which catalyzes HF etch process.

   b. Examples of S4/MacEtch;

<table>
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<tr>
<th>S4 created Ag Patterns</th>
<th>Etched Si</th>
<th>Close-up Etched Si</th>
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c. Nanowire Surface Roughening

Increasing roughening time